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High-Efficiency High-Gain 2.4 GHz Class-B Power Amplifiers in 0.13 μm CMOS for Wireless Communications

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Abstract

This paper presents high-efficiency high-gain 2.4 GHz power amplifiers (PAs) for wireless communications. Two class-B PAs are designed and verified in 0.13 μm CMOS mixed-signal/RF process provided by TSMC. The PAs employs cascode topologies with wideband multi-stage matchings. The single-stage cascode PA is designed for a high power added efficiency (PAE) of 35.4% while the gain is 20.4 dB over the -3 dB bandwidth between 2.4 GHz and 2.48 GHz. The two-stage cascode PA is targeted for a high gain of 37.7 dB while it exhibits a peak PAE of 24.1%. Supplied by 1.2 V supply voltages, the PAs consume DC powers of 4.5 mW and 9 mW, respectively.

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Keywords: Power Amplifier, Cascode, Multi-Stage, Wireless Communication

1. Introduction

In today's communication age, almost every portable device has some sort of transmitter and receiver allowing it to connect to a cellular network or available Wi-Fi networks. CMOS high-efficiency PAs are among the most challenging components in transmitter design for wireless communications, automotive radar and other applications. The main purpose of a PA design is to provide sufficiently high output power, while another very important target is to achieve high efficiency. There are several obstacles which make the implementations of a PA very difficult in CMOS technology. The use of submicron CMOS increases the difficulty of implementation due to technology limitations such as low breakdown voltage and poor transconductance. The linearity and power efficiency are lower than other technologies. However, with the trend of lower power transmitters in the next generation, implementation of CMOS PAs with good efficiencies are becoming realistic despite steadily declining field-effect transistor (FET) breakdown voltages. To improve the efficiency of the PAs, the trend is toward using class-B or class-AB topologies, which are more energy efficient compared to the class-A ones [1].

In this paper, we are going to present the designs and simulations of two class-B 2.4 GHz PAs suitable for wireless communication standard including WiMAX, Bluetooth and Wifi. The paper is organized as follows. Section 2 presents fundamentals of power amplifiers. Section 3 introduces the architectures of the proposed class-B PAs including detailed descriptions of the circuit topologies. The simulation results are presented in section 4 and conclusions are given in the last section.

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2. Power Amplifier Basics

2.1. PA Block Diagram

The general design concept of a PA is given in Fig. 1. The two port network is applied in the design consisting of two matching networks that are used on both sides of the power transistor. Maximum gain will be realized when the matching networks provide a conjugate match between the source/load impedance and the transistor impedance [2]. Specifically, the matching networks transform the input and output impedance Z_0 to the source and load impedances Z_S and Z_L, respectively. Both input and output matching network are designed for 50 Ω external load.

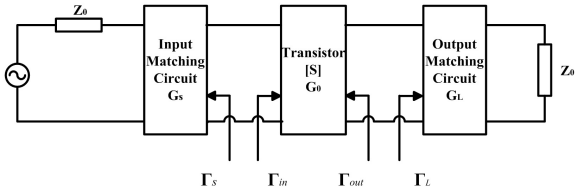

Figure 1. Block diagram of PAs.

2.2. Classification of PAs

There are generally two types of PAs: the current source mode PAs and the switching mode PAs. Different kinds of each mode of PAs and their functional principles are introduced in detail in [3]. In a current source mode PA, the power device is regarded as a current source, which is controlled by the input signal. The most important current source mode PAs are class A, class B, class AB and class C. They differ from each other in the operating points. Fig. 2 illustrates the different classes of current source mode PAs in the transfer characteristic of a FET device.

The drain current I_D exhibits pinch-off, when the channel is completely closed by the gate-source voltage V_{GS} and reaches the saturation, in which further increase of gate-source voltage results in no further increase in drain current.

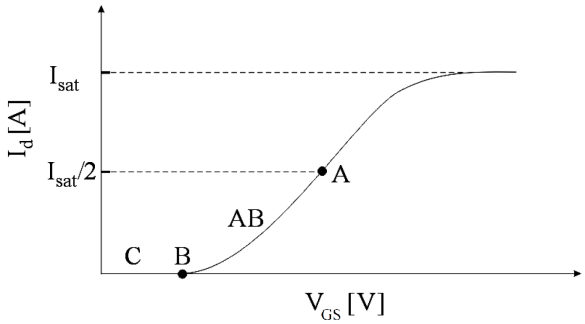

Figure 2. Operating points of the different classes of current mode PAs [4].

Table 1. Conduction angle of the different classes of current mode PAs [4]

Class	Conductance Angle
A	2π
AB	π–2π
B	π
C	0–π

The other very important concept to define the different classes of current source mode PA is the conduction angle α. The conduction angle depicts the proportion of the RF cycle for which conduction occurs. The conduction angles of different classes are summarized in table 1 while Fig. 3 shows an example of drain voltage and current waveforms in an ideal class-B PA.

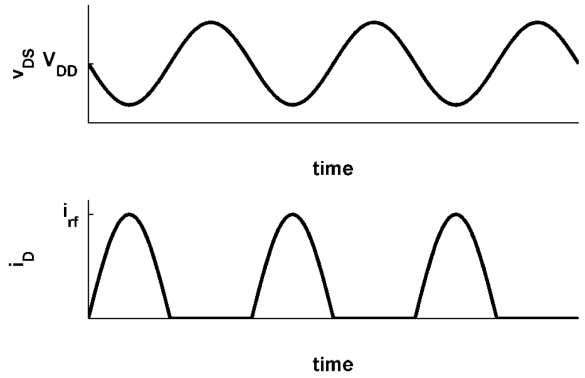

Figure 3. Drain voltage and current waveforms in an ideal class-B PA.

2.3. PA Efficiency

Efficiency is a measure of performance of a PA. The performance of a PA will be better if its efficiency is higher, irrespective of its definition. The PA is the most power-consuming block in a wireless transceiver.

Its power efficiency has a direct impact on the battery life of mobile devices. Several definitions of efficiency are commonly used with PAs. Most widely used measures are the drain efficiency and power added efficiency. The drain efficiency is defined as

$$\eta = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{DC}}} \tag{1}$$

where P_{OUT} is the RF output power at operating frequency and P_{DC} the DC power consumption of the PA output stage. It reveals how efficient the PA is when it converts the power from DC to AC. The PAE is given by

$$\mathrm{PAE} = \frac{P_{\mathrm{OUT}} - P_{\mathrm{IN}}}{P_{\mathrm{DC}}} \tag{2}$$

where P_{IN} is the input power fed to the PA and P_{DC} the total DC power consumption of the PA. The PAE gets close to η if the gain of the PA is sufficient high so that the input power is negligible.

3. Design of 2.4 GHz Class-B Power Amplifiers

The PAs are designed using the TSMC 0.13 µm CMOS mixed-signal/RF process. Its back end consists of 8 copper layers and a top aluminum redistribution layer (RDL). In order to increase the efficiency, the designed PAs are biased to operate as class-B PAs.

3.1. Single-Stage Class-B Cascode PA

Fig. 4 shows the complete circuit of the single-stage cascode PA with all component values are given in table 2. It includes an input matching network, a cascode amplifying stage and an output matching network. Apart from the capability to deliver more output power, the cascode stage alleviates the Miller effect and therefore presents wider bandwidth and better stability than common-source stage. Since PA can be stabilized by maximizing their reverse isolation, the cascode structure is employed in this design to further increase input-output reverse isolation and stability. For wideband input and output matching, multi-stage matchings using capacitors and inductors are adopted. The capacitors and inductors form 4th-order high-pass filters at input and output port. All of the capacitors also act as coupling capacitors while the DC bias voltages are applied across the inductors L_2 and L_3. On-chip inductors L_1, L_2, L_3 and L_4 have values of 1.1, 2.8, 2.4 and 0.8 nH, respectively. To operate as a class-B PA, the transistor M_1 is biased with its gate-source voltage equals to the threshold voltage, $V_{\mathrm{GS}} = V_{\mathrm{TH}} = 420$ mV. A 235 Ω resistor, R_{G}, is added in series to the gate of transistor M_1 for stabilization. The minimum-loss cascade stabilizing resistor value is determined from the Smith chart by finding the constant resistance that is tangent to the appropriate stability circle [5].

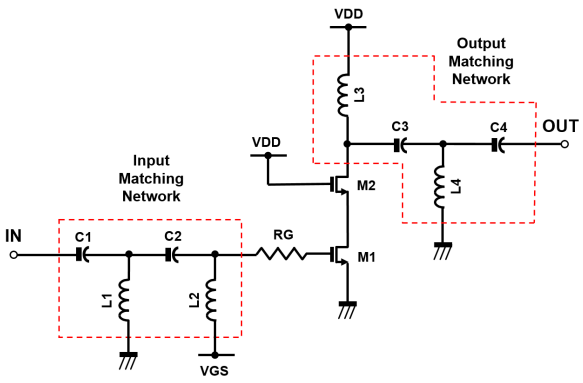

Figure 4. The single-stage class-B cascode PA.

3.2. Two-Stage Class-B Cascode PA

The single-stage PA employs four on-chip inductors in the input and output matching network for bandwidth enhancement. These inductors occupy a very large area in the layout and are hard to adapt to finer pitch technology. For two-stage

Table 2. Transistor Dimensions, Component Values and Bias Setting of Single-Stage Class-B Cascode PA

Parameter	Value
V_{DD}	1.2 V
V_{GS}	0.42 V
M_1–M_2	30 μm/130 nm
R_G	235 Ω
C_1	2.4 pF
C_2	0.8 pF
C_3	0.1 pF
C_4	1.2 pF
L_1	1.1 nH
L_2	2.8 nH
L_3	2.4 nH
L_4	0.8 nH

PA, each inductor is replaced by an equivalent transmission line (TL) for reducing chip area. Although for 2.4 GHz frequency band, the lengths of the TLs may be long. However, the long TLs can be folded for better area efficiency compared to the RF inductor counterparts.

The cross-view of the grounded coplanar waveguide transmission line (GCPW-TL) is depicted in Fig. 5. The GCPW-TL with a characteristic impedance of Z_0 of 50 Ω (the 50 Ω GCPW-TL) is used for shunt stubs of the input/output matching. Its signal line is composed of the RDL layer with a width of 9.5 μm. Ground (GND) walls composed of the 5th to 8th metal layers with a width of 2.7 μm are placed on the both side of the signal line at the distance of 7 μm. The GCPW-TL with characteristic impedance of 71 Ω (the 71 Ω GCPW-TL) is used for the shunt stubs of the inter-stage matching network. The width of the top-layer signal line is 3.2 μm, and the GND wall placed at a distance of 7.3 μm from the signal line has the width of 1.8 μm. The 2nd to 4th metal layers are meshed and stitched together with vias to form the GND plane.

Fig. 6 show the complete circuit of the two-stage cascode PA with all component values are given

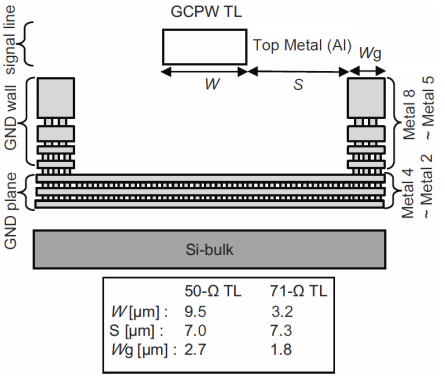

Figure 5. The cross-view of the GCPW transmission line.

in table 3. The cascode topology reduces the input capacitance of the second stage by decreasing the Miller effect due to transistor M_1. In order to double the gain, a cascade of two cascode stages is used. The capacitor C_3 blocks the DC offset of the first amplifying stage to have an independent biasing of the second amplifying stage.

The DC bias voltages are established through the transmission lines TL_2, TL_3, TL_4 and TL_5. For stabilization, the resistor R_{G1} and R_{G2} is added in series to the gate of transistor M_1 and M_3, respectively.

The lengths of the TLs and the capacitor values are determined by a nonmetric optimization process taking into account the models of MOSFETs, MOM capacitors and TLs. Many-stage amplifiers for RF frequencies tend to occupy a large area since inter-stage matching networks consist typically of several passive devices that are much large than MOSFETs.

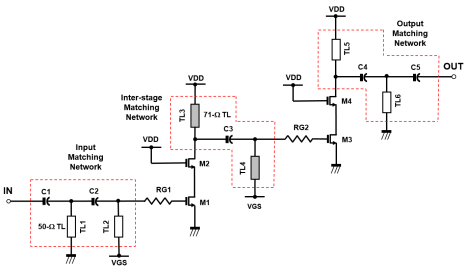

Figure 6. The two-stage class-B cascode PA.

Table 3. Transistor Dimensions, Component Values and Bias Setting of Two-Stage Class-B Cascode PA

Parameter	Value
V_{DD}	1.2 V
V_{GS}	0.42 V
M_1–M_4	30 μm/130 nm
R_{G1}–R_{G2}	235 Ω
C_1	0.56 pF
C_2	0.22 pF
C_3	0.12 pF
C_4	0.36 pF
C_5	1.15 pF
TL_1	658 μm
TL_2	1662 μm
TL_3	694 μm
TL_4	1056 μm
TL_5	936 μm
TL_6	366 μm

To realize cost-effective chips, area reduction is important. In order to reduce the area of the amplifier, the 71 Ω GCPW-TLs used in the inter-stage matching network are arranged regularly at narrow spacings, and the 71 Ω GCPW-TLs themselves are designed to be narrow, thereby reducing the footprint.

4. Simulation Results

Simulated results of the class-B PAs for TSMC 0.13 μm CMOS technology is achieved using the CADENCE design environment. Circuit design at high frequencies involves more detailed considerations than at lower frequencies when the effect of parasitic capacitances and inductances can impose serious constrains on achievable performance.

4.1. Single-Stage Class-B Cascode PA

Fig. 7 shows the simulated S-parameters of the single-stage cascode PA. S_{11} remains below -17 dB while S_{22} is less than -20 dB over a -3 dB bandwidth of 2.4–2.48 GHz. Both input and output return loss indicate relatively wideband performance.

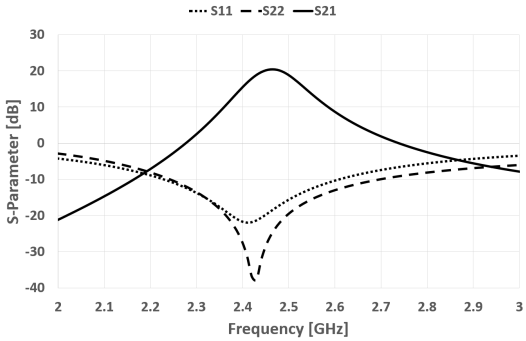

Figure 7. The simulated S-parameter of the designed single-stage PA.

The PA achieves a peak gain of 20.4 dB at 2.45 GHz while the reverse isolation is lower than -35 dB (not shown in the figure). A high reverse isolation guarantees high stability for the PA.

Fig. 8 and Fig. 9 show the drain efficiency and PAE versus input power, respectively. The designed PA obtains a peak drain efficiency of 36.6% at -10 dBm input power. It corresponds to a peak PAE of 35.4%. The linearity of the single-stage PA in term of input referred 1 dB compression point (IP1dB) is -8.8 dBm. The single-stage PA consumes only 4.5 mW from a 1.2 V supply voltage.

4.2. Two-Stage Class-B Cascode PA

Fig. 10 shows the simulated S-parameters of the two-stage cascode PA. S_{11} is less than -18 dB while S_{22} is less than -15 dB over a -3 dB bandwidth from 2.4 GHz to 2.48 GHz. The PA achieves a high gain of 37.7 dB at 2.45 GHz while the reverse isolation is lower than -35 dB. Fig. 11 and Fig. 12 show the drain efficiency and PAE versus input power, respectively. The peak drain efficiency drops to 25.4% corresponding to the peak PAE of 24.1% at –21 dBm input power. The IP1dB is -24.5 dBm. The two-stage PA consumes only 9 mW from a 1.2 V supply voltage. Table 4 summarizes the performance of the proposed PAs

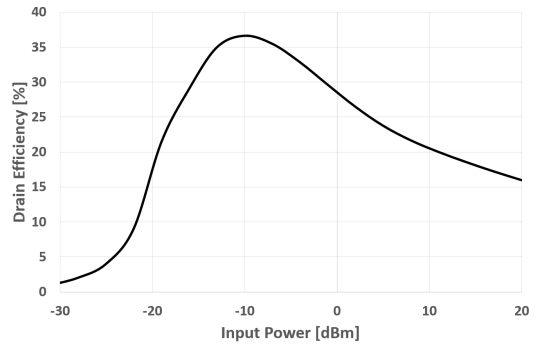

Figure 8. The simulated drain efficiency of the designed single-stage PA.

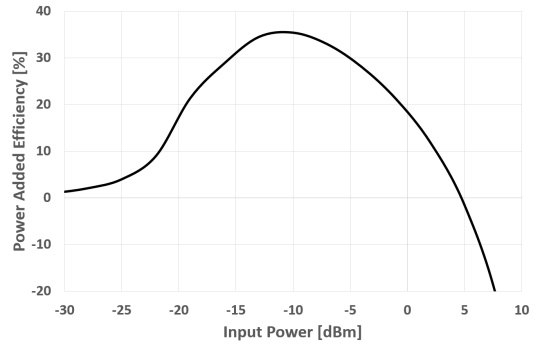

Figure 9. The simulated PAE of the designed single-stage PA.

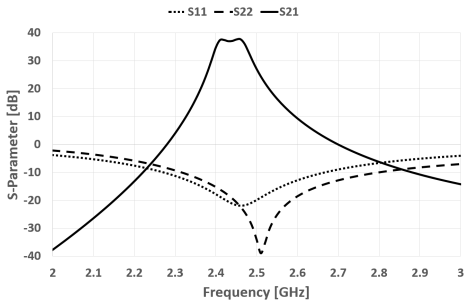

Figure 10. The simulated S-parameter of the designed two-stage PA.

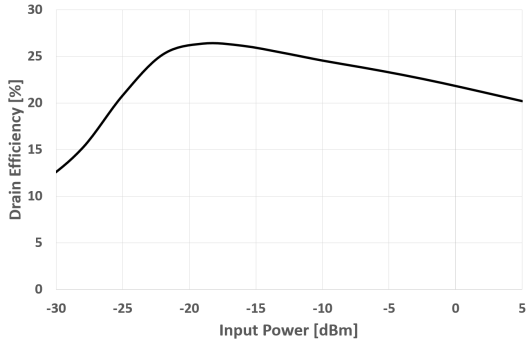

Figure 11. The simulated drain efficiency of the designed two-stage PA.

and compares them to other published designs operating in a similar frequency range. Both proposed PAs are unconditionally stable at all frequencies.

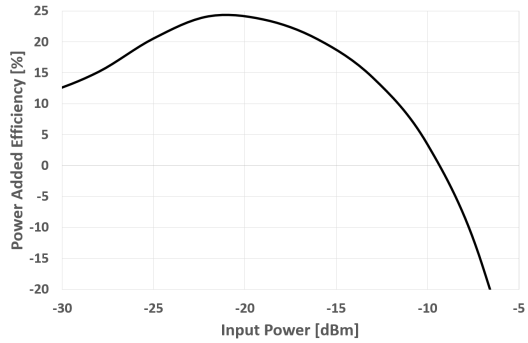

Figure 12. The simulated PAE of the designed two-stage PA.

5. Conclusions

In this paper, we have presented the design and simulation of high-efficiency high-gain 2.4 GHz PAs. Two class-B cascode PAs are designed in TSMC 0.13 μm CMOS mixed-signal/RF process. The performances of the PAs are verified by simulation results, and are competitive to other state-of-the-art PAs in CMOS. Both designed PAs are suitable for wireless communication standards including WiMAX, Bluetooth and Wifi.

Table 4. Comparison with previous published PAs operating at 2.4 GHz band

Parameter	[6]	[7]	[8]	[9]	[10]	**This work 1**	**This work 2**
CMOS technology	90 nm	65 nm	0.18 µm	0.18 µm	0.18 µm	**0.13 µm**	**0.13 µm**
Supply voltage (V)	3.3	3.3	5.6	1.8	2.4	**1.2**	**1.2**
Gain (dB)	28	32	21.4	10.4	18	**20.4**	**37.7**
Peak PAE (%)	33	25	26.1	16.2	24.6	**35.4**	**24.1**
IP1dB (dBm)	0	-7	5.6	13	7.5	**-8.8**	**-24.5**

Acknowledgement

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